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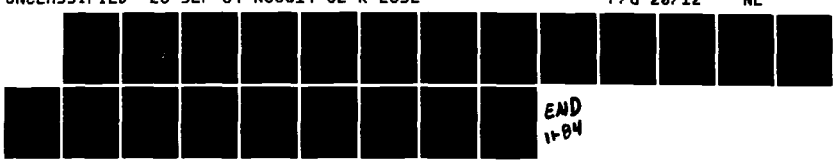

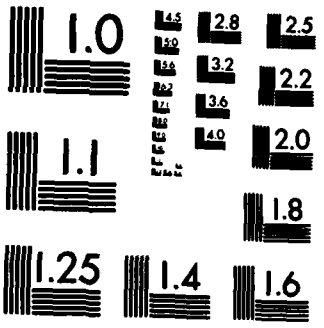

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)
The surface and interfacial charge carrier transport properties of semi-insulating InP have been investigated. It is shown that space charge limited current flow in the presence of trapping in conjunction with charge transport in the accumulation layer are present in two-terminal and three-terminal InP structures. Additional [illegible]

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Characterization of Surface Electronic Properties of Semi-Insulating InP

Annual Report for the Period: 1st May 1983 - 30th April 1984

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A-1

September 1984

Introduction

The evolution of device and integrated circuit applications of the III-V semiconductors depends, in large measure, on the achievement of a better understanding and control of the electrical properties of semi-insulating (SI) GaAs and InP. Epitaxial layers of these binary compounds and of their crystal-lattice-matched III-V ternary and quaternary alloys are grown on these SI substrates. Alternatively, direct ion implantation of donor and acceptor impurities is employed to form planar monolithic integrated circuits. In either case the devices are embedded or reside upon their respective semi-insulating substrates whose bulk and surface properties affect the properties of discrete and integrated circuit transistors and optical electronic circuits. Fluctuations in device parameters on a chip and inter-chip variations must be controlled or at least understood sufficiently so that they can be taken into account if large scale integrated (LSI) circuits based on GaAs and InP are to be accepted for performing functions which cannot be done by means of existing and available technologies within acceptable trade-offs in processing, performance and cost.

A great deal of time, effort and money has been spent in producing high quality SI GaAs containing few residual impurities and a low free carrier concentrations. Much effort is being spent worldwide at present on processing low dislocation density SI boules of GaAs and processing these into wafers for substrates. Considerably less effort has been spent thus far on producing pure SI InP. The problem appears to be associated with residual donor impurities, of the order of $10^{15}/cm^3$, in pure InP. These might probably be phosphorous point defects although a clear and definitive identification has yet to be made. In any case, a high concentration of Fe deep-level acceptor impurities is required to compensate these donors. These impurities have a

significant effect on the electrical properties of bulk and SI InP. They are, therefore, of particular importance in the accumulation-type metal-insulator-semiconductor field effect transistors[1] (MISFET) whose parameters are strongly dependent on the surface properties of SI InP. It is to be expected, furthermore, that these traps will have a substantial effect on the threshold for "sidegating" and "backgating" which represent a parasitic interaction between adjacent transistors and sets specific limits, therefore, on LSI, and they may also affect the channel electron mobility and the dynamic response of such MISFET.

Two-Terminal Current vs Voltage Measurements

In order to make a variety of current vs voltage (i-V) measurements on bare (i.e. uncoated) SI InP surfaces as well as on surfaces coated with dielectric layers, (such as those used as gate insulators in insulated gate field effect transistors) a computer controlled system such as that shwon in Fig. 1 was assembled. It consists of a programmable power supply (HP 6034A) controlled by a HP-87XM microcomputer. The potential applied to the specimen is stepped in preset increments through the desired range, allowing adequate time for the current through it to reach a stable value. The current is determined by monitoring the voltage developed across a small resistance R (much smaller than that of the specimen) by means of a Keithley 177 Microvolt Digital multimeter whose output is read by the computer. The stored V-i data can then be plotted subsequently by the computer.

FE-doped SI InP with chemo-mechanically polished <100> surfaces had its electron density determined from Hall measurements (assuming single band electronic conduction) to be $n \approx 10^8/cm^3$ and mobility $\mu \approx 1.5^3 x 10^2 cm/$ /V-sec determined from resistivity measurements. Photolithographic techniques were

then used to delineate rectangular contacts made by alloying Au-Ge (in accordance with the method described in the enclosed publication) using various interelectrode spacings. One specimen with ion implanted contacts with an interelectrode spacing of 2 μm, made at NOSC was also measured and yielded essentially similar results. Although the contact resistance of the ion-implanted contacts is lower than that of Au-Ge alloyed electrodes their qualitative i-V characteristics (described subsequently) are the same.

Space Charge-limited Currents in SI InP

The experimentally derived i-V data shown in Fig. 2 are similar to those usually measured on SI GaAs. However, to our knowledge this is the first evidence that SI InP has an i-V characteristic in which space charge limited currents (SCLC) may play significant roles similar to those observed on SI GaAs[2]. Theoretical interpretations based on charge transport in insulators in which SCLC is dominant are based on the simultaneous solution of Poisson's equation and the continuity equation[3]. In low electric fields the current is a linear function of the applied voltage because the free electron density present in the insulator is much greater than that of the electric field-dependent injected electrons from the contacts. As the injected electron density becomes dominant the current takes on a quadratic dependence on the applied voltage and is proportional to the inverse of the interelectrode separation to the third power. If deep level traps within the vicinity of the Fermi level are present then charge transport associated with trap filling is much more complicated[4]. Beyond the linear i-V region the current rises nonlinearly with voltage up to a value such that all the available traps which can be charged are filled. Thereafter the current rises steeply with an incremental increase in V up to a value where further increases in voltage

exhibit the quadratic dependence of i on V predicted for the trap free-case[5]. The threshold voltage for the trap-filled space-charge-limited current rise, V_{TFL}, is of particular importance because it coincides with the onset of parasitic coupling between an "ohmic" contact made to SI GaAs and an adjacent metal-semiconductor field effect transistor (MESFET) on the same SI substrate, i.e. SCLC measured between two contacts have an V_{TFL} whose magnitude is essentially identical to the threshold for "sidegating" modulation of the drain current of a MESFET and probably a MISFET by a potential applied to a neighboring electrode. In SI GaAs a trapping mediated SCLC model such as that described by Lampert and Mark[4] was introduced by a number of investigators in an attempt to explain their experimental measurements[6]. However, two major problems arose in attempting to fit the experimentally measured i-V data to the model. It was found that the calculated V_{TFL} is about one order of magnitude greater than that measured and that its dependence on interelectrode spacing is linear rather than quadratic. While the introduction of a surface depletion region and a change in sign of the free carriers beneath it induced, presumably, by thermal annealing can provide[6] a fit to the experimentally measured i-V data, the validity of this model and its applicability to SI GaAs remains in doubt.

In at least some respects the situation is more favorable in the case of SI InP, as shown by the curve in Fig. 2. It was calculated using the Lampert-Mark model[7] with the measured electron density and mobility from Hall effect and resistivity data by assuming that the dominant trap level is Fe^{3+} located at ~0.6 eV below the conduction band minimum. Although the experimentally measured and calculated i vs V curves are in very good agreement and the calculated Fe^{3+} acceptor density, which is of the order of $\sim 10^{16}/cm^3$, is in fair agreement[8] with the Fe concentration measured on similar SI InP

specimens using secondary ion mass spectrometry, we have not been able, as yet, to confirm the expected quadratic dependence of V_{TFL} on the interelectrode spacing. Furthermore, there is a serious question whether one-dimensional current flow is sufficient to explain experimental observations such as described in our enclosed paper. A two-dimensional SCLC model was developed by Geurst[9] and may be applicable to the planar type of structures we are involved with. Furthermore, it does predict a linear dependence of the threshold voltage on the interelectrode spacing such as observed experimentally. However, we have not explored as yet its specific applicability to two-terminal i-V measurements made on SI InP. A more realistic SCLC model for SI InP and its role in device and integrated circuit functions remains to be made as part of our current and future efforts characterizing SI InP.

Conclusions

1. We have demonstrated[10] that in high electric fields SCLC in SI InP plays a significant role in two-terminal devices with uncoated (bare) surfaces.
2. We have demonstrated that in two-terminal devices with a dielectric coated surface as well as in accumulation type MISFET, SCLC, in conjunction with accumulation charge transport, plays a significant role.
3. We have demonstrated that trap-mediated SCLC is a significant factor in surface charge transport of SI InP.
4. We believe that relatively small changes in surface potential in either two-terminal or in three terminal accumulation mode devices can have a significant effect on charge transport.
5. We have not been able as yet to show a direct correlation between the time dependence of the current observed on dielectric-coated SI InP and the current instability observed on accumulation type MISFET.

6. We find that the time dependent drain current drift following the application of a step function potential to the gate of a long channel accumulation MISFET is a function of the nature of its gate dielectric layer.

Open-ended Issues

a) It is not clear as yet what (if any) role SCLC has in accumulation type MISFET in limiting its frequency response which is an order of magnitude smaller then that of depletion mode MISFET.

b) The contact resistance and spreading resistance of accumulation mode MISFETs needs to be determined and its effect on their dynamic range and gain-bandwidth products remain to be determined.

c) The correlation between V_{TFL} and the thresholds for sidegating and backgating in MISFET and JFET made on SI InP and parasitic coupling between devices made on a common SI InP substrate remain to be determined.

d) No direct a correlation has yet been established between the long time constants described in the enclosed publication and drift and instabilities of the drain current.

These are the specific issues slated for further investigation at UCSD. Perhaps the most significant issue is that of understanding the nature and characteristics of the dielectric - InP interface and major emphasis will be placed upon it.

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Figure 1. Block diagram of computer controlled current vs voltage measurements used to determine space-charge-limited current flow and trapping in semi-insulating InP.

Figure 2. Log-log plot of the current vs voltage dependence of uncoated (bare) surfaces of SI InP with Au-Ge eutectic electrodes spaced 5μm from each other. The electron density $n = 6.6 \times 10^7/cm^3$. The concentration of Fe impurities calculated from this curve (assuming Fe^{3+} to be the main trap level) is $7.89 \times 10^{15}/cm^3$. Points represent experimental measurements, curve is calculated i-V relation using Mark-Lampert model. $V_{TFL} \simeq 36V$ and linear region is shown by straight line.

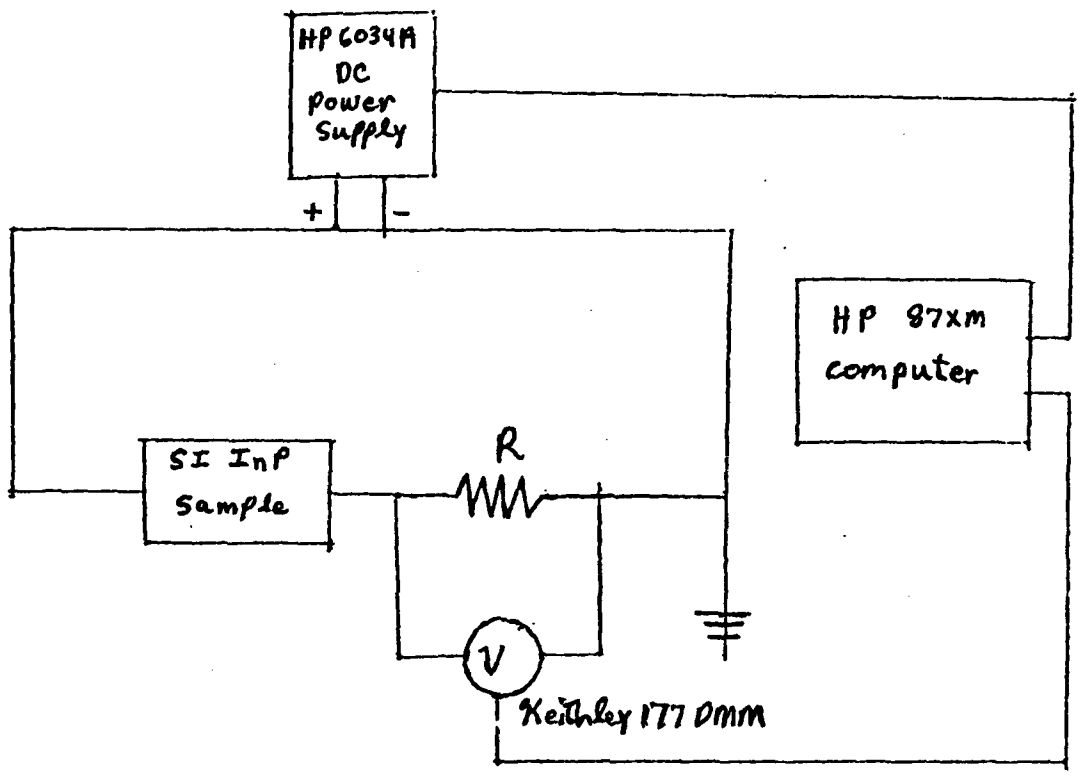
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Fig.1

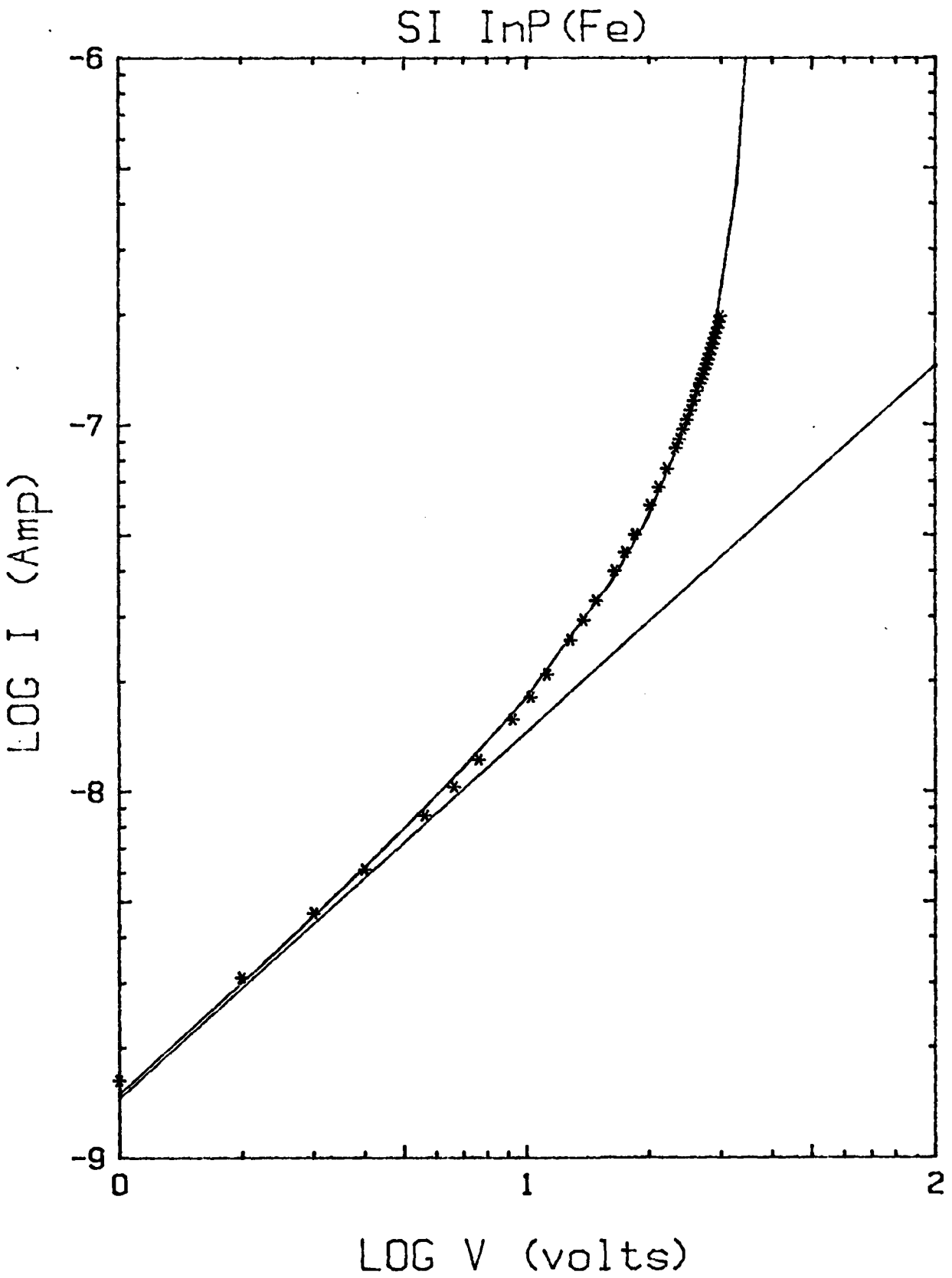

FIG. 2

Surface properties of semi-insulating indium phosphide[a)]

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Electrical measurements on two-terminal structures and on A-MISFET's, with 20 and 30 μm long channels, fabricated on SiO_2 or Al_2O_3 coated semi-insulating InP, indicate that charge transport between their Au–Ge eutectic contacts takes place by a combination of electron transport in the accumulation layer and space charge limited current flow, both affected by deep level traps. Following application of a step voltage, the total time dependence current may be described qualitatively by $I(t) = I_0 \exp(-t/\tau_2) + I_1[1 - \exp(-t/\tau_1]$, where $\tau_2 \gg \tau_1$ and I_0 is the accumulation current.

PACS numbers: 73.60.Fw, 73.30. + y

I. INTRODUCTION

Semi-insulating (SI) InP shows considerable technological promise as a substrate for making planar, monolithic, integrated circuits using metal–insulator–semiconductor field effect transistors (MISFET's). It may also prove to be a viable substrate for electro-optic integrated circuits employing injection electroluminescent lasers, photodiodes, and phototransistors made of ternary and quaternary III–V alloys having lattice constants compatible with InP.

Bulk, Czochralski grown, single crystal, SI InP is produced by compensating its residual shallow donors with deep level Fe^+ acceptor impurities. It is n type at room temperature with a typical electron density $n \simeq 10^8$ cm^{-3}, mobility $\mu \simeq 3 \times 10^3$ cm^2 V^{-1} s^{-1}, and typical bulk resistivity of the order of 10^7 Ω cm.

SI InP surfaces coated with a synthetic dielectric such as SiO_2 or Al_2O_3 exhibit surface accumulation[1] with an equilibrium surface Fermi level $E_F^* \simeq 0.16$ eV. This is essentially the same as that of n-type, (100)-oriented InP which is slightly depleted, and is in good agreement[2–5] with the barrier height and surface Fermi level of (110)-and (100)-oriented "free" surfaces obtained by x-ray photoemission spectroscopic methods.

Modulation of the surface potential in accumulation by a positive potential applied to the gate of a SI InP MISFET is feasible. Such accumulation mode transistors[6] (A-MISFET's) are of particular importance for use as enhancement type devices in high frequency and low power microwave integrated circuits.[7] The significance of surface transport of charge carriers in SI InP is, therefore, self-evident. However, relatively little is known about either the bulk or surface transport of charge in SI InP. The bulk properties of SI InP may, in some respects, be similar to those of SI GaAs. It appears that both are affected by charge injection at the contacts, by space-charge-limited (SCL) current flow, and by trapping some of the injected charge carriers.[8,9] Nonetheless, their surface properties are likely to be quite different because of the different energy levels of the surface states, which determine the equilibrium position of their surface Fermi levels[1]—near midgap for GaAs and near the conduction band edge for InP.

This paper presents preliminary two-terminal and three-terminal electrical measurements made on SI InP. A tentative interpretation of the data is offered which proposes that surface transport consists of SCL current affected by trapping, combined with electron transport in the surface accumulation layer.

II. EXPERIMENTAL

Devices were fabricated on $\sim 10^7$ Ω cm, (100)-oriented, Fe doped, SI InP which had been chemomechanically polished in a bromine–methanol solution, cleaned in hot acetone, rinsed in methanol, given a detergent scrub, and deionized water rinse. Drain-source windows were produced photolithographically, following which Au–Ge eutectic was deposited by thermal evaporation. After removal of the photoresist, these contacts were annealed at 375 °C for 15 min and the current versus voltage linearity determined. Thereafter, an ~ 0.1 μm thick SiO_2 or Al_2O_3 layer was deposited by rf plasma-assisted chemical vapor deposition procedures at 300 °C. Alternatively, the insulating layer was deposited[10] immediately following the contacts, then the anneal was performed as before. The contact pads are rectangular, 0.5 mm $\times$ 1 mm (the narrow edge fronting the channel) with either a 20 μm long or a 30 μm long channel between them.

A-MISFET (i.e., three terminal devices) were made by the vacuum deposition of an Al gate over the channel between the source and drain pads, using photolithographic procedures to delineate the gate contour. Gate current leakage, at 1 V, was found to be negligible, on the order of 10^{-11} A.

III. ELECTRICAL MEASUREMENTS

The insert in Fig. 1 shows that the current I is, to good approximation, a linear function of the applied voltage V between Au–Ge eutectic alloy contacts made to SI InP, prior to deposition of a SiO_2 layer. For much higher values of V or much smaller interelectrode spacing, I has a power law dependence on V consistent with SCL current flow in the presence of traps.[8] Rose[11] has shown that a linear I vs V regime precedes SCL current flow if the density of injected charge carriers is much smaller than that of the thermally generated carriers (or that contributed by ionized impurities).

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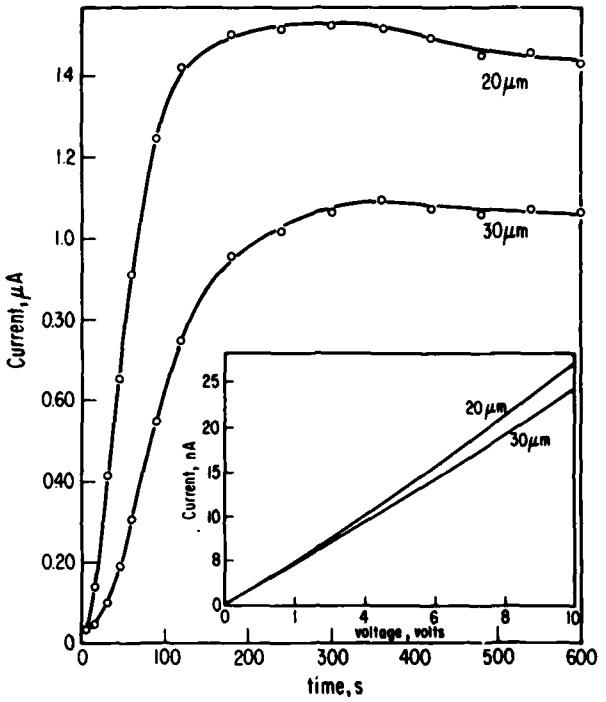

FIG. 1. Current vs time for two-terminal SI InP structures after SiO_2 surface coating is applied; potential difference $V = 4.8$ V; two interelectrode spacings: 20 and 30 μm. Insert shows typical two-terminal structure current–voltage characteristics prior to deposition of SiO_2. Same interelectrode spacings as above.

Figure 1 also shows that following the deposition of an SiO_2 layer over the same SI InP specimens, the current measured at a constant voltage, applied in the form of a step function, has acquired a time dependence: It rises to a quasi-steady-state plateau and then decays much more slowly. The peak currents are some two orders of magnitude greater than currents measured between the same contacts prior to deposition of the SiO_2. This current depends on the interelectrode spacing.

From curves similar to those in Fig. 1, it was determined that the current plateau is a function of V^{α}, where $\alpha > 2$, and commonly is ~ 4. On the other hand, it was found that the time constant τ of the rise of $I(t)$ is essentially independent of V. Removal of the SiO_2 layer from the InP surface eliminates the time-dependent evolution of I and restores the linear I–V characteristic shown in the insert.

It is proposed here that the surface charge carrier transport in SI InP, up to and including the plateau in $I(t)$ shown in Fig. 1, proceeds by a combination of SCL current flow in the presence of traps, and the motion of free electrons in the surface accumulation layer. Their relative contributions may vary, depending on the free carrier concentration. Meiners and Wider[12] have shown that the equilibrium surface potential of SiO_2 coated SI InP, with $n = 2.2 \times 10^8$ cm^{-3} is $Vs = 0.39$ V, in accumulation. Thus a small accumulation current may exist even in the absence of an applied gate voltage if a potential difference is applied to such a two-terminal structure. The SCL current may be derived from the first order assumption that the time dependent electron density n is described by

$$\frac{dn}{dt} = \frac{n_s - n}{\tau_1}.$$

n_s is the total steady-state electron density and τ_1 is the time constant required for the electric field and electron density to reach steady state. n_s is the sum of the initial (time = 0) electron density n_0 due to the accumulation layer, and the steady-state SCL density n_1. Thus, the above equation may be written as

$$\frac{dn}{dt} = \frac{(n_0 + n_1) - n}{\tau_1} \tag{1}$$

with solution,

$$n = n_0 + n_1(1 - e^{-t/\tau_1}). \tag{2}$$

By assuming the electron mobility to be time and position independent, the time dependent current becomes

$$I(t) = I_0 + I_1(1 - e^{-t/\tau_1}). \tag{3}$$

This is essentially a first order approximation to the total current, consisting of the superposition of a current I_0, a function of the free electron density n_0 in the accumulation layer, and a SCL current, with a time dependent electron density expressed by the second term in Eq. (2). Relations similar to Eq. (3) have been deduced by Baron *et al.*[13] for double injection SCL current measurements made on bulk Si biased in the square law Mott–Gurney SCL regime,[8] and by Dean[14] for SCL measurements made on p-type InSb.

Figure 2 illustrates the time and gate-voltage dependent evolution of the source-drain current I_{DS} of a three-terminal (A-MISFET) structure. Its two-terminal properties were qualitatively in accord with those shown in Fig. 1. For a constant V_{DS} of 5 V, i_{DS} was recorded as a function of time for various values of the gate voltage V_G. The data can be fitted by means of Eq. (3) for each value of V_G. In addition, since I_0 is assumed to be the accumulation current in the channel of the A-MISFET, and provided $I_0 = I_{DSS}$, then the saturated current of the surface accumulation channel,

$$I_0 = K(V_G - V_T)^2 \tag{4}$$

as shown by Wieder.[15] V_T is a threshold voltage and the constant of proportionality K is a function of C_{in} (the capacitance per unit area of the gate insulator), the channel length l and width z, and of the electron field effect mobility μ such that

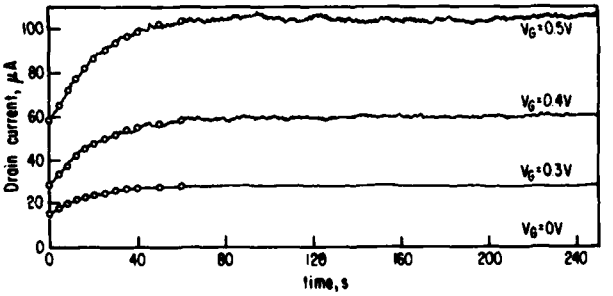

FIG. 2. Drain current vs time as a function of gate voltage V_G for an A-MISFET with SiO_2 gate insulator and 20 μm long channel. Drain-source potential is 5 V. Circles represent least-square fit of data to Eq. (3) using $\tau_1 \simeq 20$ s.

$$K = C_{in}\mu z/2l. \tag{5}$$

In accordance with Eq. (4), Fig. 3 shows that $I_0^{1/2}$ is a linear function of V_G, at least down to gate voltage comparable to V_T. The slope of $I_0^{1/2}$ vs V_G yields K, and assuming the dielectric constant of the SiO_2 layer is 3.9, the field effect mobility $\mu \simeq 900\ cm^2/V\ s$, a value consistent[6,16] with that determined on A-MISFET of smaller dimensions using either Au–Ge or ion-implanted source and drain contacts.

In Fig. 2, no decay of $I(t)$ is evident, in contrast to experimental data obtained on A-MISFET's of smaller dimensions[6,16] but in accordance with $I(t)$ in Fig. 1, for $t<300$ s. Figure 4, on the other hand, shows that an A-MISFET of the same dimensions as that which yielded Fig. 2, but having an Al_2O_3 gate insulating layer of comparable thickness, concurs with the measurements made on smaller devices[16]: $I(t)$ is dominated by the decay following an initial rise to its peak value I_0. The origin of I_0 is again assumed to be due to surface accumulation.

If the decay in $I(t)$ is attributed to the charging of traps with a very long time constant τ_2, then with Q_t being the trapped charge (assumed to be zero initially),

$$\frac{dQ_t}{dt} + \frac{Q_t}{\tau_2} - I_0 = 0 \tag{6}$$

from which may be obtained a time dependent current of the form,

$$I(t) = \frac{dQ_t}{dt} = I_0\, e^{-t/\tau_2}. \tag{7}$$

Figure 4 demonstrates that experimental data can be roughly fitted to this expression. Figure 5 indicates that this device, too, yields the expected linear dependence of $I_0^{1/2}$ on V_G.

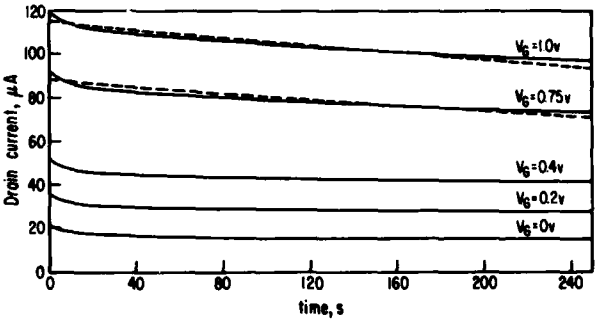

FIG. 4. Drain current vs time as a function of gate voltage V_G for a A-MISFET with Al_2O_3 gate insulator and 20 μm long channel. Drain-source potential is 5 V. Dashed lines represent least-square fit of data to Eq. (7) using $\tau_2 \simeq 960$ s.

It is thought that more generally, the current may be expressed as a superposition of Eqs. (3) and (7) as

$$I(t) = I_1(1 - e^{-t/\tau_1}) + I_0 e^{-t/\tau_2}. \tag{8}$$

It may be seen that Eqs. (3) and (7) are special cases of Eq. (8), which depend upon the relative contributions of the accumulation SCL, and trapping mechanisms. Returning for a moment to Fig. 1, one may see that both the SCL current rise, and, at longer time, the trap-related decay are in evidence, in qualitative agreement with Eq. (8).

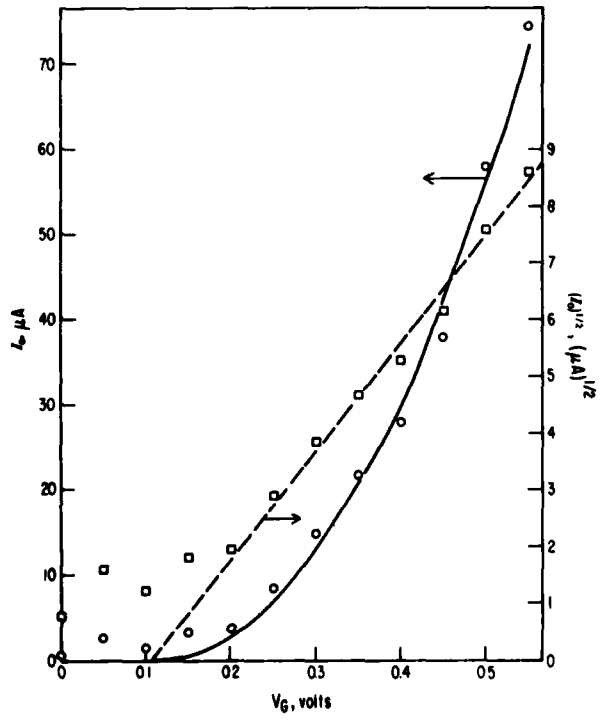

FIG. 3. Saturated drain current I_0 vs V_G (circles) and $I_0^{1/2}$ vs V_G (squares) for same sample as Fig. 2. Solid curve represents least-square fit of data to Eq. (4) with $K \simeq 380\ \mu A/V^2$ and $V_T \simeq 0.1$ V.

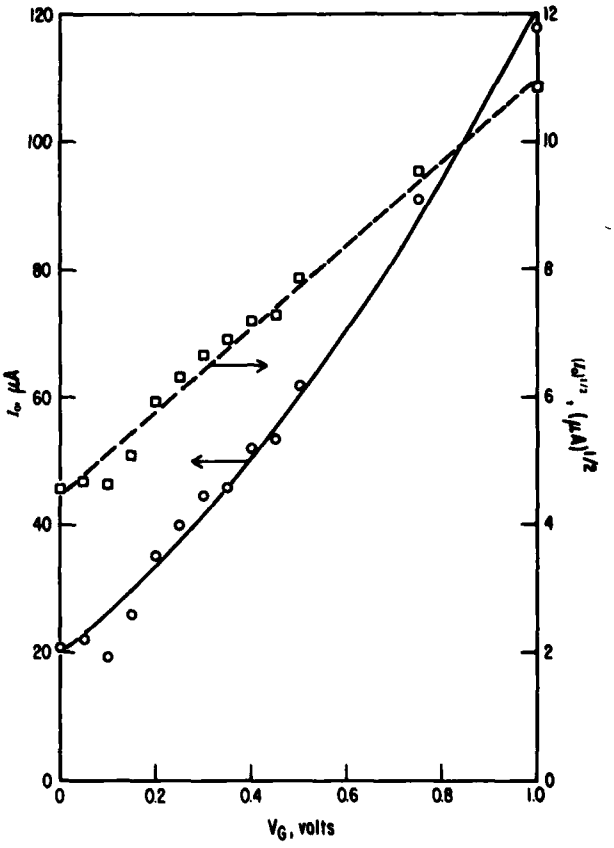

FIG. 5. Saturated drain current I_0 vs V_G (circles) and $I_0^{1/2}$ vs V_G (squares) for same sample as Fig. 4. Solid curve represents least-square fit of data to Eq. (4) with $K = 43\ \mu A/V^2$ and $V_T = -0.7$ V.

IV. DISCUSSION

From the data herein presented, it appears that SCL currents may contribute a significant fraction of the current flowing in the surface of dielectric-coated SI InP in weak accumulation and small to moderate applied electric fields. It is premature as yet to try to develop a model of the combined accumulation and SCL current flows. The data presented here suggest that the SCL current flow occurs in the SI material underneath the accumulated layer. However, the possibility that SCL currents may flow in the native oxide beneath the synthetic dielectric layer cannot be ruled out. No contribution is expected from currents flowing in the synthetic dielectric itself. In large electric fields, such as produced in $\sim 0.5\,\mu$m long channels, I is a quadratic function of V as expected for the trap-filled limit of SCL currents.[8] However, no consistent data of this type has been obtained as yet for the larger devices used here.

SCL theory[11,17] also indicates that an increase in the free carrier concentration relative to trapped carriers might be expected to yield an increase in the steady state SCL current and a decrease in τ_1. It was found that a two-terminal device, on a SI InP specimen which had been annealed at 675 °C in a P_2 overpressure for 10 min prior to deposition of the SiO_2 layer or formation of the contacts, had a somewhat larger $I(t)$ and a τ_1 value smaller by roughly an order of magnitude compared to those of Fig. 1. There also resulted a greatly accentuated decrement in $I(t)$ beyond its peak value. These changes may be due to an increase in the free electron density in the vicinity of the surface produced by redistribution of the Fe^+ acceptors which compensate the residual shallow donors. Oberstar[18] *et al.* have found that following the annealing of SI InP at 800 °C for 30 min, the Fe concentration at room temperature, as measured by SIMS (secondary ion mass spectroscopy) decreased by more than one order of magnitude from its original value within 0.8 μm of the surface. This is also consistent with the measurement of Shanabrook[19] *et al.* which indicates that annealing at 730 °C for 15 min increased the free electron density of SI InP by more than an order of magnitude. Annealing at such temperatures is a common practice following ion implantation, but more data will be required to establish an unambiguous correlation between the anneal and the SCL current parameters.

An alternative explanation to trapping for the decay of $I(t)$ following its peak is presented as a model for slow current drift in A-MISFET's. In this model, developed by Goodnick[20] *et al.*, electrons from the InP channel tunnel thermionically to a conducting In_2O_3 layer within the native oxide, under the influence of the gate potential. The data in Fig. 4 can be fitted by this model as well. It is, however, not yet evident how such a mechanism might affect the decay of $I(t)$ in two-terminal structures such as described here.

ACKNOWLEDGMENTS

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Surface properties of semi-insulating indium phosphide[a)]

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Electrical measurements on two-terminal structures and on A-MISFET's, with 20 and 30 μm long channels, fabricated on SiO_2 or Al_2O_3 coated semi-insulating InP, indicate that charge transport between their Au–Ge eutectic contacts takes place by a combination of electron transport in the accumulation layer and space charge limited current flow, both affected by deep level traps. Following application of a step voltage, the total time dependence current may be described qualitatively by $I(t) = I_0 \exp(-t/\tau_2) + I_1[1 - \exp(-t/\tau_1]$, where $\tau_2 \gg \tau_1$ and I_0 is the accumulation current.

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I. INTRODUCTION

Semi-insulating (SI) InP shows considerable technological promise as a substrate for making planar, monolithic, integrated circuits using metal–insulator–semiconductor field effect transistors (MISFET's). It may also prove to be a viable substrate for electro-optic integrated circuits employing injection electroluminescent lasers, photodiodes, and phototransistors made of ternary and quaternary III–V alloys having lattice constants compatible with InP.

Bulk, Czochralski grown, single crystal, SI InP is produced by compensating its residual shallow donors with deep level Fe^+ acceptor impurities. It is n type at room temperature with a typical electron density $n \simeq 10^8$ cm^{-3}, mobility $\mu \simeq 3 \times 10^3$ cm^2 V^{-1} s^{-1}, and typical bulk resistivity of the order of 10^7 Ω cm.

SI InP surfaces coated with a synthetic dielectric such as SiO_2 or Al_2O_3 exhibit surface accumulation[1] with an equilibrium surface Fermi level $E_F^s \simeq 0.16$ eV. This is essentially the same as that of n-type, (100)-oriented InP which is slightly depleted, and is in good agreement[2–5] with the barrier height and surface Fermi level of (110)-and (100)-oriented "free" surfaces obtained by x-ray photoemission spectroscopic methods.

Modulation of the surface potential in accumulation by a positive potential applied to the gate of a SI InP MISFET is feasible. Such accumulation mode transistors[6] (A-MISFET's) are of particular importance for use as enhancement type devices in high frequency and low power microwave integrated circuits.[7] The significance of surface transport of charge carriers in SI InP is, therefore, self-evident. However, relatively little is known about either the bulk or surface transport of charge in SI InP. The bulk properties of SI InP may, in some respects, be similar to those of SI GaAs. It appears that both are affected by charge injection at the contacts, by space-charge-limited (SCL) current flow, and by trapping some of the injected charge carriers.[8,9] Nonetheless, their surface properties are likely to be quite different because of the different energy levels of the surface states, which determine the equilibrium position of their surface Fermi levels[1]—near midgap for GaAs and near the conduction band edge for InP.

This paper presents preliminary two-terminal and three-terminal electrical measurements made on SI InP. A tentative interpretation of the data is offered which proposes that surface transport consists of SCL current affected by trapping, combined with electron transport in the surface accumulation layer.

II. EXPERIMENTAL

Devices were fabricated on $\sim 10^7$ Ω cm, (100)-oriented, Fe doped, SI InP which had been chemomechanically polished in a bromine–methanol solution, cleaned in hot acetone, rinsed in methanol, given a detergent scrub, and deionized water rinse. Drain-source windows were produced photolithographically, following which Au–Ge eutectic was deposited by thermal evaporation. After removal of the photoresist, these contacts were annealed at 375 °C for 15 min and the current versus voltage linearity determined. Thereafter, an ~ 0.1 μm thick SiO_2 or Al_2O_3 layer was deposited by rf plasma-assisted chemical vapor deposition procedures at 300 °C. Alternatively, the insulating layer was deposited[10] immediately following the contacts, then the anneal was performed as before. The contact pads are rectangular, 0.5 mm $\times$ 1 mm (the narrow edge fronting the channel) with either a 20 μm long or a 30 μm long channel between them.

A-MISFET (i.e., three terminal devices) were made by the vacuum deposition of an Al gate over the channel between the source and drain pads, using photolithographic procedures to delineate the gate contour. Gate current leakage, at 1 V, was found to be negligible, on the order of 10^{-11} A.

III. ELECTRICAL MEASUREMENTS

The insert in Fig. 1 shows that the current I is, to good approximation, a linear function of the applied voltage V between Au–Ge eutectic alloy contacts made to SI InP, prior to deposition of a SiO_2 layer. For much higher values of V or much smaller interelectrode spacing, I has a power law dependence on V consistent with SCL current flow in the presence of traps.[8] Rose[11] has shown that a linear I vs V regime precedes SCL current flow if the density of injected charge carriers is much smaller than that of the thermally generated carriers (or that contributed by ionized impurities).

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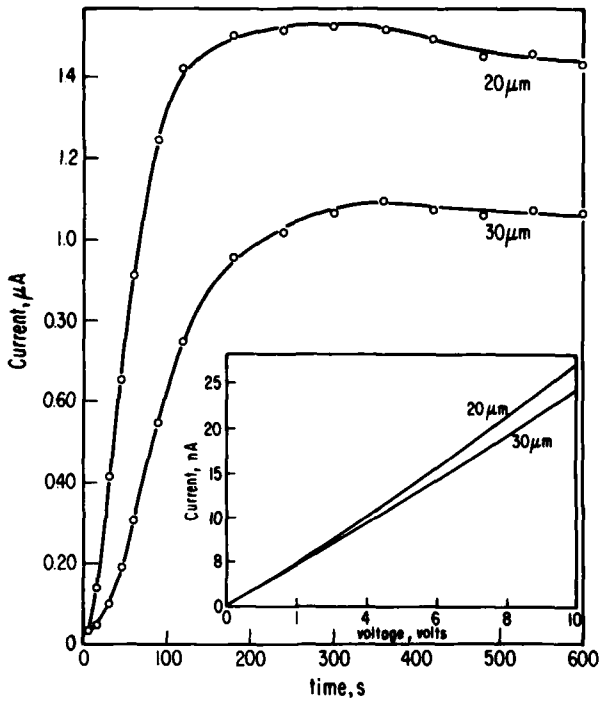


FIG. 1. Current vs time for two-terminal SI InP structures after SiO_2 surface coating is applied; potential difference $V = 4.8$ V; two interelectrode spacings: 20 and 30 μm. Insert shows typical two-terminal structure current–voltage characteristics prior to deposition of SiO_2. Same interelectrode spacings as above.

Figure 1 also shows that following the deposition of an SiO_2 layer over the same SI InP specimens, the current measured at a constant voltage, applied in the form of a step function, has acquired a time dependence: It rises to a quasi-steady-state plateau and then decays much more slowly. The peak currents are some two orders of magnitude greater than currents measured between the same contacts prior to deposition of the SiO_2. This current depends on the interelectrode spacing.

From curves similar to those in Fig. 1, it was determined that the current plateau is a function of V^{α}, where $\alpha > 2$, and commonly is ~ 4. On the other hand, it was found that the time constant τ of the rise of $I(t)$ is essentially independent of V. Removal of the SiO_2 layer from the InP surface eliminates the time-dependent evolution of I and restores the linear I–V characteristic shown in the insert.

It is proposed here that the surface charge carrier transport in SI InP, up to and including the plateau in $I(t)$ shown in Fig. 1, proceeds by a combination of SCL current flow in the presence of traps, and the motion of free electrons in the surface accumulation layer. Their relative contributions may vary, depending on the free carrier concentration. Meiners and Wider[12] have shown that the equilibrium surface potential of SiO_2 coated SI InP, with $n = 2.2 \times 10^8$ cm^{-3} is $Vs = 0.39$ V, in accumulation. Thus a small accumulation current may exist even in the absence of an applied gate voltage if a potential difference is applied to such a two-terminal structure. The SCL current may be derived from the first order assumption that the time dependent electron density n is described by

$$\frac{dn}{dt} = \frac{n_s - n}{\tau_1}.$$

n_s is the total steady-state electron density and τ_1 is the time constant required for the electric field and electron density to reach steady state. n_s is the sum of the initial (time = 0) electron density n_0 due to the accumulation layer, and the steady-state SCL density n_1. Thus, the above equation may be written as

$$\frac{dn}{dt} = \frac{(n_0 + n_1) - n}{\tau_1} \tag{1}$$

with solution,

$$n = n_0 + n_1(1 - e^{-t/\tau_1}). \tag{2}$$

By assuming the electron mobility to be time and position independent, the time dependent current becomes

$$I(t) = I_0 + I_1(1 - e^{-t/\tau_1}). \tag{3}$$

This is essentially a first order approximation to the total current, consisting of the superposition of a current I_0, a function of the free electron density n_0 in the accumulation layer, and a SCL current, with a time dependent electron density expressed by the second term in Eq. (2). Relations similar to Eq. (3) have been deduced by Baron *et al.*[13] for double injection SCL current measurements made on bulk Si biased in the square law Mott–Gurney SCL regime,[8] and by Dean[14] for SCL measurements made on p-type InSb.

Figure 2 illustrates the time and gate-voltage dependent evolution of the source-drain current I_{DS} of a three-terminal (A-MISFET) structure. Its two-terminal properties were qualitatively in accord with those shown in Fig. 1. For a constant V_{DS} of 5 V, i_{DS} was recorded as a function of time for various values of the gate voltage V_G. The data can be fitted by means of Eq. (3) for each value of V_G. In addition, since I_0 is assumed to be the accumulation current in the channel of the A-MISFET, and provided $I_0 = I_{DSS}$, then the saturated current of the surface accumulation channel,

$$I_0 = K(V_G - V_T)^2 \tag{4}$$

as shown by Wieder.[15] V_T is a threshold voltage and the constant of proportionality K is a function of C_{in} (the capacitance per unit area of the gate insulator), the channel length l and width z, and of the electron field effect mobility μ such that

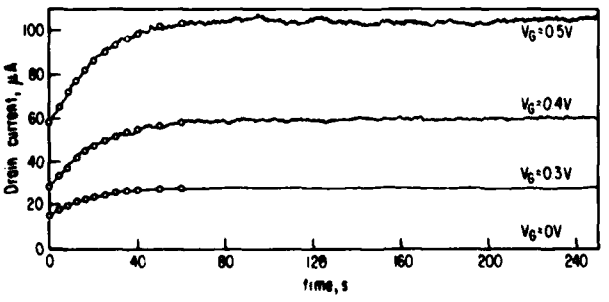


FIG. 2. Drain current vs time as a function of gate voltage V_G for an A-MISFET with SiO_2 gate insulator and 20 μm long channel. Drain-source potential is 5 V. Circles represent least-square fit of data to Eq. (3) using $\tau_1 \simeq 20$ s.

$$K = C_{in}\mu z/2l. \tag{5}$$

In accordance with Eq. (4), Fig. 3 shows that $I_0^{1/2}$ is a linear function of V_G, at least down to gate voltage comparable to V_T. The slope of $I_0^{1/2}$ vs V_G yields K, and assuming the dielectric constant of the SiO_2 layer is 3.9, the field effect mobility $\mu \simeq 900\ cm^2/V\ s$, a value consistent[6,16] with that determined on A-MISFET of smaller dimensions using either Au–Ge or ion-implanted source and drain contacts.

In Fig. 2, no decay of $I(t)$ is evident, in contrast to experimental data obtained on A-MISFET's of smaller dimensions[6,16] but in accordance with $I(t)$ in Fig. 1, for $t < 300$ s. Figure 4, on the other hand, shows that an A-MISFET of the same dimensions as that which yielded Fig. 2, but having an Al_2O_3 gate insulating layer of comparable thickness, concurs with the measurements made on smaller devices[16]: $I(t)$ is dominated by the decay following an initial rise to its peak value I_0. The origin of I_0 is again assumed to be due to surface accumulation.

If the decay in $I(t)$ is attributed to the charging of traps with a very long time constant τ_2, then with Q_t being the trapped charge (assumed to be zero initially),

$$\frac{dQ_t}{dt} + \frac{Q_t}{\tau_2} - I_0 = 0 \tag{6}$$

from which may be obtained a time dependent current of the form,

$$I(t) = \frac{dQ_t}{dt} = I_0\, e^{-t/\tau_2}. \tag{7}$$

Figure 4 demonstrates that experimental data can be roughly fitted to this expression. Figure 5 indicates that this device, too, yields the expected linear dependence of $I_0^{1/2}$ on V_G.

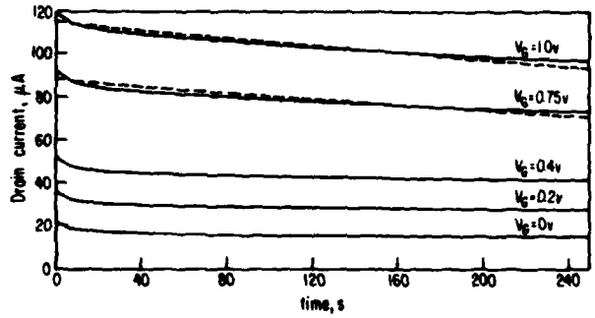
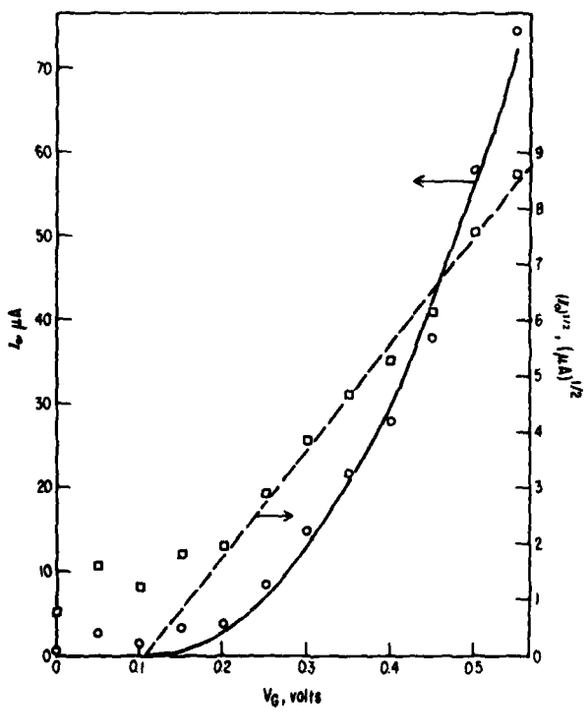


FIG. 4. Drain current vs time as a function of gate voltage V_G for a A-MISFET with Al_2O_3 gate insulator and 20 μm long channel. Drain-source potential is 5 V. Dashed lines represent least-square fit of data to Eq. (7) using $\tau_2 \simeq 960$ s.

It is thought that more generally, the current may be expressed as a superposition of Eqs. (3) and (7) as

$$I(t) = I_1(1 - e^{-t/\tau_1}) + I_0 e^{-t/\tau_2}. \tag{8}$$

It may be seen that Eqs. (3) and (7) are special cases of Eq. (8), which depend upon the relative contributions of the accumulation SCL, and trapping mechanisms. Returning for a moment to Fig. 1, one may see that both the SCL current rise, and, at longer time, the trap-related decay are in evidence, in qualitative agreement with Eq. (8).



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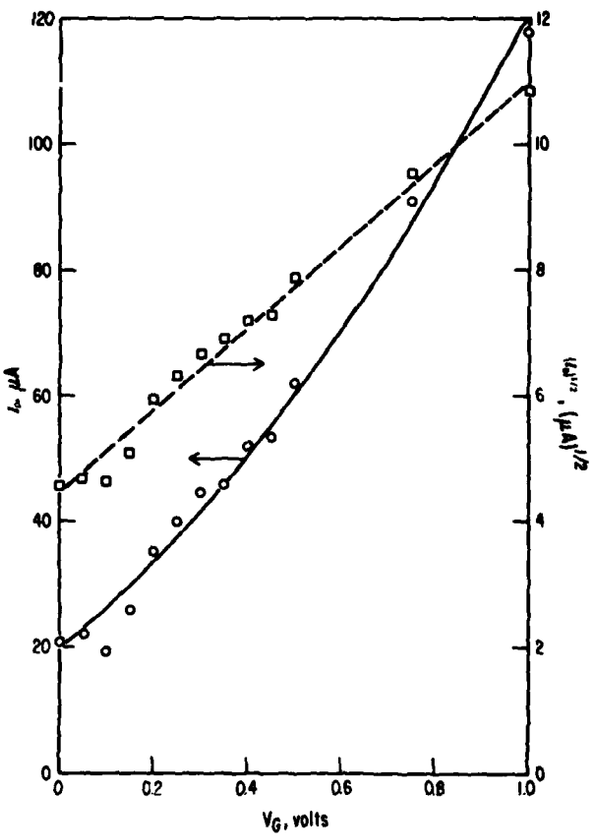

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